LISTING OF THE CLAIMS:

Claim 1 (Currently Amended) A method of ~~improving the SiGe bipolar yield of~~ fabricating a SiGe heterojunction bipolar transistor comprising the steps of:

providing a heterojunction bipolar transistor structure comprising at least an underlying SiGe base region, an insulator layer formed on surface portions of said underlying SiGe base region, and an emitter formed on said insulator layer and in contact with said underlying SiGe base region through an emitter opening formed in said insulator layer, said emitter, said insulator layer and said SiGe base region each having exposed sidewalls;

forming a permanent passivation layer on said exposed sidewalls of said emitter, said insulator layer and portions of said SiGe base region; and

siliciding exposed silicon surfaces of at least said emitter and said SiGe base region not protected by said permanent passivation layer to form silicide regions therein, wherein said permanent passivation layer prevents bridging between silicide regions thereby substantially eliminating shorts and improving bipolar yield by as much as 20-30%.

Claim 2 (Original) The method of Claim 1 wherein said passivation layer is formed from a rapid thermal chemical vapor deposition process.

Claim 3 (Original) The method of Claim 1 wherein said passivation layer is composed of a nitride, an oxide, an oxynitride or any combination thereof.

Claim 4 (Original) The method of Claim 1 wherein said passivation layer is a nitride passivation layer.

Claim 5 (Original) The method of Claim 4 wherein said nitride passivation layer is formed from a rapid thermal chemical vapor deposition process which is carried out in a nitrogen-containing atmosphere.

Claim 6 (Original) The method of Claim 5 wherein said nitrogen-containing atmosphere is selected from the group consisting of NO, N_2O and N_2.

Claim 7 (Previously Presented) The method of Claim 2 wherein said rapid thermal chemical vapor deposition process is carried out at a temperature of about 700°C or greater.

Claim 8 (Original) The method of Claim 1 wherein said SiGe base region is formed by a deposition process selected from the group consisting of ultra-high vacuum chemical vapor deposition (UHVCVD), molecular beam epitaxy (MBE), rapid thermal chemical vapor deposition (RTCVD) and plasma-enhanced chemical vapor deposition.

Claim 9 (Currently Amended) A SiGe heterojunction bipolar transistor comprising:

a semiconductor substrate having a collector and subcollector region located therein, wherein said collector is located between isolation regions that are also present in the substrate;

a SiGe layer atop said substrate, said SiGe layer including polycrystalline Si regions positioned above said isolation regions and a SiGe base region located above said collector and subcollector regions;

a patterned insulator layer atop said SiGe base region, said patterned insulator having an opening therein;

an emitter located on said patterned insulator layer and in contact with said SiGe base region through said opening, said emitter, said patterned insulator layer and said SiGe base region each having exposed sidewalls;

a permanent conformal passivation layer positioned on said exposed sidewalls of said emitter, said patterned insulator layer and a portion of said SiGe base region; and

silicide regions located on exposed portions of said SiGe layer, including portions of said SiGe base region, and said emitter not covered by said permanent conformal passivation layer, wherein said permanent passivation layer prevents bridging between silicide regions thereby substantially eliminating shorts and improving bipolar yield by as much as 20-30%.

Claim 10 (Original) The SiGe heterojunction bipolar transistor of Claim 9 wherein said semiconductor substrate is selected from the group consisting of Si, Ge, SiGe, GaAs, InAs, InP, other III/V compound semiconductors, Si/Si and Si/SiGe.

Claim 11 (Original) The SiGe heterojunction bipolar transistor of Claim 9 wherein said emitter is composed of intrinsic polysilicon.

Claim 12 (Original) The SiGe heterojunction bipolar transistor of Claim 9 wherein said patterned insulator is composed of SiO_2 or Si oxynitride.

Claim 13 (Original) The SiGe heterojunction bipolar transistor of Claim 9 wherein said patterned insulator is composed of multi-insulator layers.

Claim 14 (Original) The SiGe heterojunction bipolar transistor of Claim 9 wherein said passivation layer is also formed on vertical sidewalls of said patterned insulator and portions of said SiGe base region.

Claim 15 (Original) The SiGe heterojunction bipolar transistor of Claim 9 wherein said silicide regions are formed in an exposed horizontal surface of said emitter, said polycrystalline Si region and a portion of said SiGe base region.

Claim 16 (Original) The SiGe heterojunction bipolar transistor of Claim 9 wherein said passivation layer is composed of a nitride, an oxide, an oxynitride or any combination thereof.

Claim 17 (Original) The SiGe heterojunction bipolar transistor of Claim 9 wherein said passivation layer is a nitride passivation layer.

Claim 18 (Currently Amended) A SiGe heterojunction bipolar transistor comprising:

a semiconductor substrate having a collector and subcollector region located therein, wherein said collector is located between isolation regions that are also present in the substrate;

a SiGe layer atop said substrate, said SiGe layer including polycrystalline Si regions positioned above said isolation regions and a SiGe base region located above said collector and subcollector regions;

a patterned insulator layer atop said SiGe base region, said patterned insulator having an opening therein;

an emitter located on said patterned insulator layer and in contact with said SiGe base region through said opening, said emitter, said patterned insulator layer and said SiGe base region each having exposed sidewalls;

a permanent conformal passivation layer positioned on said exposed sidewalls of said emitter, said patterned insulator layer and an inclined portion of said SiGe base region; and

silicide regions located on exposed portions of said SiGe layer, including portions of said SiGe base region, and said emitter not covered by said permanent conformal passivation layer, wherein said permanent passivation layer prevents bridging between silicide regions thereby substantially eliminating shorts and improving bipolar yield by as much as 20-30%.